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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
LOTTICH, JOSHUA P	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,495	MCDONALD-MAIER ET AL.	
	Examiner	Art Unit	
	JOSHUA P. LOTTICH	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-31 and 33-38* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 22-26 and 32-38 are objected to because of the following informalities:

2. In claim 22, the claim is dependent upon itself. For the purpose of this examination, the examiner presumes that it is dependent upon claim 21.

3. In claims 25, “the signal conversion means" has no antecedent basis in the claims. For the purpose of this examination, the examiner presumes that it should read "the signal conversion arrangement”.

4. In claims 32-38, the claims are numbered 22-28. For the purpose of this examination, the examiner presumes that they should read claims 32-38.

5. In claim 32, “periphery of an 30 upper surface” should read “periphery of an upper surface”.

6. In claim 35, 37, and 38, the claims are dependent upon claims 24, 26, and 27 respectively. This is unclear as they are not further limiting an integrated circuit, but a set of integrated circuits and a method of performing a debug operation, respectively. For the purpose of this examination, the examiner presumes that claims 35, 37, and 38 are dependent upon claims 34, 36, and 37, respectively.

7. Appropriate correction is required.

8. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims

are presented, they must be numbered **consecutively** beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 22-28 been renumbered 32-38.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 21, 22, 25, 26, and 33-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Kantz et al. (U.S. Patent Application Publication No. 2001/0043078), referred hereinafter “Kantz”.

11. Regarding claim 21, Kantz disclose(s) an integrated circuit assembly (semiconductor chip 1, fig. 1, [0039]) for use in a system,

wherein the integrated circuit assembly is configurable as a production part (for fabrication the solar cell, used for testing, is removed from the circuit assembly, [0011, 0047], fig. 4), or as a development part (test configuration, [0008-0011]),

wherein the assembly comprises:

a first arrangement of connection terminals for connecting the integrated circuit to other components of the system (semiconductor chip 1, fig. 1, necessarily has terminals or pins that connect it to a system. Examiner notes that if the solar cells used for testing

are removed for manufacture [0011, 0047], fig. 4, then there must be another set of connections for connecting to a system);

debug circuitry (self test unit 2, fig. 1, [0039-0042]); and

a debug interface comprising a second arrangement of connection terminals (semiconductor laser generating optical radiation pulses 41, fig. 1, 3, [0042, 0046])

wherein for the development part configuration of the integrated circuit assembly, the second arrangement of connection terminals is adapted to be connected to a signal conversion arrangement for converting electrical signals provided to the second arrangement of terminals into a format for transmission (generate optical radiation pulses 41 in accordance with data to be transmitted, [0042]) to external monitoring circuitry (external test device, [0002], external test unit, [0004, 0008], external evaluation device, [0020], receiver 5, [0042, 0043]) using a communications link (UV light or laser, [0023, 0042], fig. 1), and

wherein for the production part configuration of the integrated circuit assembly, the second arrangement of connection terminals is adapted such that no communications link is provided from the second arrangement of terminals to external monitoring circuitry (for fabrication the solar cell 30, used for testing, is removed from the circuit assembly, [0011, 0047], fig. 4, which means that the semiconductor laser, see above, will have no power source until the chip 1 is connected to a system and thus after the chips have been cut from the wafer there is no communication link, via the semiconductor laser, to an external tester), and

wherein debug support resources (programmable memory units 9, fig. 1, [0040]) of the integrated circuit assembly are accessed by the first arrangement of connection terminals (Given that the self-test unit 2 stores repair information in programmable memory units 9 about which memory cells are defective and thus in need of redundant memory cells, those memory locations must be accessed when connected to a system so that only non-defective cells are accessed).

12. Regarding claim 22, Kantz disclose(s) wherein the signal conversion arrangement comprises electro-optical conversion means (generate optical radiation pulses 41 in accordance with data to be transmitted, [0042]), and

the communications link comprises an optical communications line (UV light or laser, [0023, 0042], fig. 1).

13. Concerning claim(s) 36, given the structure of Kantz, the claimed method step(s) would inherently be performed when using the system disclosed by Kantz, in claim(s) 22, as discussed above, and therefore is(are) rejected under 35 U.S.C. 102(b).

14. Regarding claim 25, Kantz disclose(s) wherein the integrated circuit assembly (semiconductor chip 1, fig. 1, 3, 5a, and 5b) comprises, for both the development part configuration and the production part configuration, the signal conversion means (given that the semiconductor laser is in the functional unit 4, [0023, 0042], and thus is not cut away during fabrication, [0047], fig. 4, the laser is a part of both the development and production part configuration).

15. Regarding claim 26, Kantz disclose(s) wherein the signal conversion means is integrated into a monolithic circuit (functional unit 4, fig. 1, [0042]) of the integrated circuit assembly (semiconductor chip 1, fig. 1).

16. Regarding claim 33, Kantz disclose(s) a second integrated circuit memory device (nonvolatile memory unit 7, fig. 1, [0044]),

comprising a third arrangement of connection terminals (as seen in fig. 1, memory 7 is connected to functional unit 4) connected to the first (terminal EX, fig. 1, [0044]) or second arrangement of connection terminals of the first integrated circuit,

wherein the debug interface provides access to internal operation information of the first and second integrated circuits (the test data DA, which contains information about the performance of the chip test, [0042], is read out from memory 7, [0044]).

17. Regarding claim 34, Kantz disclose(s) a set of integrated circuits, comprising:

at least one first integrated circuit assembly as claimed in any preceding claim configured as a development part (see rejections of claims 21, 22, 25, and 26 above); and

a plurality of second integrated circuit assemblies as claimed in claim 1 configured as production parts having the same design as the at least one first assembly in respect of the first arrangement of connection terminals and the debug interface (given the rejection of claim 1, see above, and that the semiconductor chips of Kantz are made from semiconductor wafer 10, [0004, 0047], there would be a plurality of production configured parts having the same design as the first assembly, except no

solar cells for powering testing (i.e. the terminals for connection to a system and the debug interface would be the same)), and

wherein the plurality of second assemblies are not provided with the communications link of the at least one first assembly (for fabrication the solar cell 30, used for testing, is removed from the circuit assembly, [0011, 0047], fig. 4, which means that the semiconductor laser, see above, will have no power source until the chip 1 is connected to a system and thus after the chips have been cut from the wafer there is no communication link, via the semiconductor laser, to an external tester).

18. Regarding claim 35, Kantz disclose(s) wherein the plurality of second integrated circuit assemblies have the same design as the at least one first assembly in respect of the debug circuitry (the self test unit (BIST) 2, [0042, 0043], fig. 1, is internal to semiconductor chip 1, fig. 1, thus it will be the same when diced from the wafer 10, [0011, 0047], fig. 4).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

21. Claims 23, 28-30, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz as applied to claims 21, 22, and 36 above, and in view of White et al. (U.S. Patent No. 6,331,782), referred hereinafter "White".

22. Regarding claim(s) 23, Kantz disclose(s) the apparatus as set forth above.

23. Kantz do(es) not expressly disclose wherein the electro-optical conversion means comprises an array of lasers, but does, however, disclose wherein the electro-optical conversion means comprises a laser (semiconductor laser generating optical radiation pulses 41, fig. 1, 3, [0042, 0046]).

24. White teach(es) that it is known in the art wherein the electro-optical conversion means comprises an array of lasers (col. 5, ln. 34-42).

25. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the system of Kantz by including the lasers as taught by White.

26. One of ordinary skill would have been motivated to make the combination, in order to provide improved testability of the device without requiring extra input and output pins (col. 2, ln. 21-23, White), since by having more output lasers it would allow for more detailed test information to be transmitted, thus improving the depth and detail of the testing.

27. Concerning claim(s) 37, the combination, in claim(s) 23, as discussed above, renders the claimed method step(s) obvious since such would be the logical manner of using the combination, and therefore is(are) rejected under 35 U.S.C. 103(a).

28. Regarding claim 28, White also disclose(s) wherein the signal conversion arrangement comprises analogue electrical circuitry for implementing digital communication over the communications link (test circuit portion 70 converts electrical signals into electromagnetic radiation that corresponds to those signals, where the radiation is a radio-frequency (RF), col. 5, ln. 7-33, fig. 5).

29. Regarding claim 29, White also disclose(s) wherein the signal conversion arrangement comprises analogue electrical circuitry for providing a control signal for controlling an electro-optical conversion means (the test information may be encoded onto an infrared beam or modulated or encoded onto a beam of optical radiation (light), col. 5, ln. 34-42, the encoding would necessitate a control signal or signals).

30. Regarding claim 30, White also disclose(s) wherein the first arrangement of connection terminals are provided as a ring of terminals around the periphery of an upper surface of the assembly (contact pads 64, fig. 5, col. 4, ln. 63 – col. 5, ln. 6), and

the second arrangement of connection terminals are provided on the upper surface of the assembly within the ring (test circuitry 70 is included in the circuit and the lasers, col. 5, ln. 34-42, or the RF transmitter, col. 5, ln. 24-33, are located on top of the die, within the ring, fig. 5, in order to communicate to the probe 50, located above the chip as seen in fig. 1, 4, and 7, col. 5, ln. 43-50).

31. Claims 24 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz in view of White as applied to claims 23 and 37 above, and further in view of Walter Schottky Institute Research ("Long Wavelength Surface Emitting Lasers: Introduction", http://web.archive.org/web/20030707154500/www.wsi.tum.de/E26/en/research/vcsel/index.htm), referred hereinafter "Schottky".

32. Regarding claim(s) 24, Kantz as modified by White disclose(s) the apparatus as set forth above.

33. Kantz as modified by White do(es) not expressly disclose wherein the lasers comprise vertical cavity surface emitting lasers (VCSELs).

34. Schottky teach(es) that it is known in the art wherein the lasers comprise vertical cavity surface emitting lasers (p. 1 of pdf, last two paragraphs and p. 2, fig. 1).

35. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the system of Kantz as modified by White by including the VCSELs as taught by Schottky.

36. One of ordinary skill would have been motivated to make the combination, because VCSELs have low electric power consumption, a capability for on-wafer testing, and a simplified fiber coupling and packaging (p. 1, last paragraph, Schottky).

37. Concerning claim(s) 38, the combination, in claim(s) 24, as discussed above, renders the claimed method step(s) obvious since such would be the logical manner of using the combination, and therefore is(are) rejected under 35 U.S.C. 103(a).

38. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz, as applied to claim 21 above, in view of Birdsley et al. (U.S. Patent No. 6,850,081), referred hereinafter “Birdsley”.

39. Regarding claim(s) 27, Kantz disclose(s) the apparatus as set forth above.

40. Kantz do(es) not expressly disclose wherein the development part configuration is provided with the signal conversion arrangement and the production part configuration is not provided with the signal conversion arrangement.

41. Birdsley teach(es) that it is known in the art wherein the development part configuration is provided with the signal conversion arrangement (laser diode 230 is connected to the package 210 for testing via external tester 250, col. 4, ln. 38-49, fig. 3) and the production part configuration is not provided with the signal conversion arrangement (the laser diode 230 is not part of the package 210 (i.e. when not being tested, the device has no signal conversion arrangement), col. 4, ln. 38-49, fig. 3).

42. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the system of Kantz by including the signal conversion arrangement for development and production differing as taught by Birdsley.

43. One of ordinary skill would have been motivated to make the combination, in order to allow for testing to be performed at a remote location from the tester (col. 3, ln. 44-47), meaning that since the laser diode is not integrated into the circuit it allow for more freedom and flexibility in testing arrangements and less space taken up on the circuit itself.

44. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz in view of White, as applied to claim 30 above, and further in view of Robertsson et al. (U.S. Patent No. 6,343,164), referred hereinafter "Robertsson".

45. Regarding claim(s) 31, Kantz as modified by White disclose(s) the apparatus as set forth above.

46. Kantz as modified by White do(es) not expressly disclose wherein the second arrangement of terminals are formed from a top metal layer of the assembly.

47. White do(es) however disclose(s) wherein the second arrangement of terminals are on the top of the assembly (test circuitry 70 is included in the circuit and the lasers, col. 5, ln. 34-42, or the RF transmitter, col. 5, ln. 24-33, are located on top of the die, within the ring, fig. 5, in order to communicate to the probe 50, located above the chip as seen in fig. 1, 4, and 7, col. 5, ln. 43-50).

48. Robertsson teach(es) that it is known in the art wherein the second arrangement of terminals are formed from a top metal layer of the assembly (contact pads 59 for electrically contacting the laser chip 7 ... are formed by the top metal layer 41, col. 4, ln. 34-58, fig. 4).

49. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the system of Kantz as modified by White by including the top metal layer as taught by Robertsson.

50. One of ordinary skill would have been motivated to make the combination, in order to align and electrically connect to the laser chip (col. 4, ln. 34-58).

Allowable Subject Matter

51. Claim 32 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSHUA P. LOTTICH whose telephone number is (571)270-3738. The examiner can normally be reached on M-Th 7:30am-5pm, Alternating Fridays 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marc Duncan/
Primary Examiner, Art Unit 2113

Marc Duncan
Examiner
Art Unit 2113

/J. P. L./
Examiner, Art Unit 2113